

Features

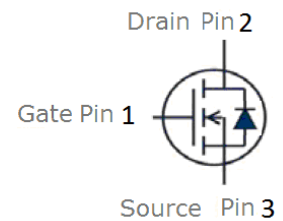
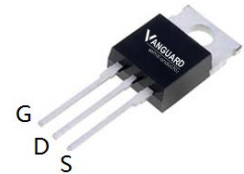
- Enhancement mode
- Low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- VitoMOS[®] II Technology
- 100% Avalanche test
- Pb-free lead plating; RoHS compliant



Part ID	Package Type	Marking	Tape and reel information
VST009N06MS-G	TO-220AB	009N06MG	50pcs/Tube

V_{DS}	60	V
$R_{DS(on),TYP} @ V_{GS}=10\text{ V}$	8	m Ω
$R_{DS(on),TYP} @ V_{GS}=4.5\text{ V}$	13	m Ω
I_D	60	A

TO-220AB



Maximum ratings, at $T_A = 25^\circ\text{C}$, unless otherwise specified

Symbol	Parameter	Rating	Unit	
$V_{(BR)DSS}$	Drain-Source breakdown voltage	60	V	
V_{GS}	Gate-Source voltage	± 20	V	
I_S	Diode continuous forward current	$T_C = 25^\circ\text{C}$	60	A
I_D	Continuous drain current @ $V_{GS}=10\text{V}$	$T_C = 25^\circ\text{C}$	60	A
		$T_C = 100^\circ\text{C}$	43	A
I_{DM}	Pulse drain current tested ①	$T_C = 25^\circ\text{C}$	240	A
I_{DSM}	Continuous drain current @ $V_{GS}=10\text{V}$	$T_A = 25^\circ\text{C}$	11	A
		$T_A = 70^\circ\text{C}$	9	A
E_{AS}	Avalanche energy, single pulsed ②	16	mJ	
P_D	Maximum power dissipation	$T_C = 25^\circ\text{C}$	60	W
P_{DSM}	Maximum power dissipation ③	$T_A = 25^\circ\text{C}$	2	W
$T_{STG,TJ}$	Storage and Junction Temperature Range	-55 to 175	$^\circ\text{C}$	

Thermal Characteristics

Symbol	Parameter	Typical	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.5	3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	75	$^\circ\text{C/W}$

Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Static Electrical Characteristics @ T_j=25°C (unless otherwise stated)						
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	60	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =60V, V _{GS} =0V	--	--	1	μA
	Zero Gate Voltage Drain Current (T _j =125°C)	V _{DS} =60V, V _{GS} =0V	--	--	100	μA
I _{GSS}	Gate-Body Leakage Current	V _{GS} =±20V, V _{DS} =0V	--	--	±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.3	1.8	2.5	V
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =10V, I _D =30A	--	8	11	mΩ
		T _j =100°C	--	11	--	mΩ
R _{DS(on)}	Drain-Source On-State Resistance ④	V _{GS} =4.5V, I _D =20A	--	13	17	mΩ
Dynamic Electrical Characteristics @ T_j = 25°C (unless otherwise stated)						
C _{iss}	Input Capacitance	V _{DS} =30V, V _{GS} =0V, f=1MHz	865	1155	1535	pF
C _{oss}	Output Capacitance		440	585	780	pF
C _{rss}	Reverse Transfer Capacitance		10	20	30	pF
R _g	Gate Resistance	f=1MHz	0.1	0.9	5	Ω
Q _{g(10V)}	Total Gate Charge	V _{DS} =30V, I _D =30A, V _{GS} =10V	--	20	27	nC
Q _{g(4.5V)}	Total Gate Charge		--	9.7	13	nC
Q _{gs}	Gate-Source Charge		--	4.6	6.1	nC
Q _{gd}	Gate-Drain Charge		--	3.7	5.6	nC
Switching Characteristics						
T _{d(on)}	Turn-on Delay Time	V _{DD} =30V, I _D =30A, R _G =3Ω, V _{GS} =10V	--	8.4	--	ns
T _r	Turn-on Rise Time		--	59	--	ns
T _{d(off)}	Turn-Off Delay Time		--	18	--	ns
T _f	Turn-Off Fall Time		--	44	--	ns
Source- Drain Diode Characteristics @ T_j = 25°C (unless otherwise stated)						
V _{SD}	Forward on voltage	I _{SD} =30A, V _{GS} =0V	--	0.9	1.2	V
T _{rr}	Reverse Recovery Time	T _j =25°C, I _{sd} =30A, V _{GS} =0V	--	20	40	ns
Q _{rr}	Reverse Recovery Charge	di/dt=100A/μs	--	8.5	17	nC

NOTE: ① Repetitive rating; pulse width limited by max junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.1mH, R_G = 25Ω, I_{AS} = 18A, V_{GS} = 10V. Part not recommended for use above this value

③ The power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C.

④ Pulse width ≤ 380μs; duty cycles ≤ 2%.

Typical Characteristics

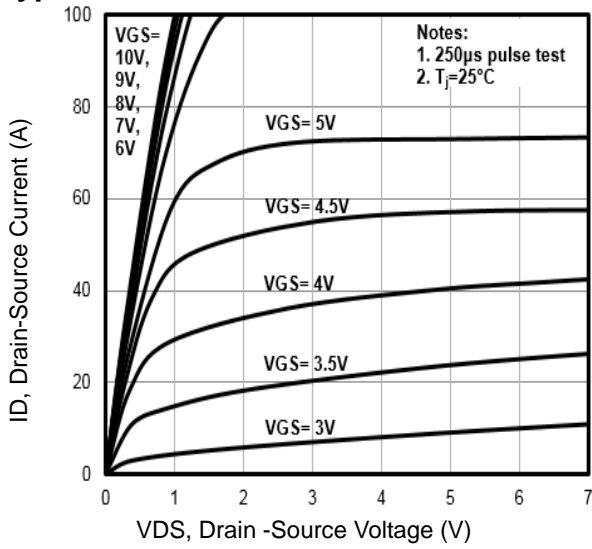


Fig1. Typical Output Characteristics

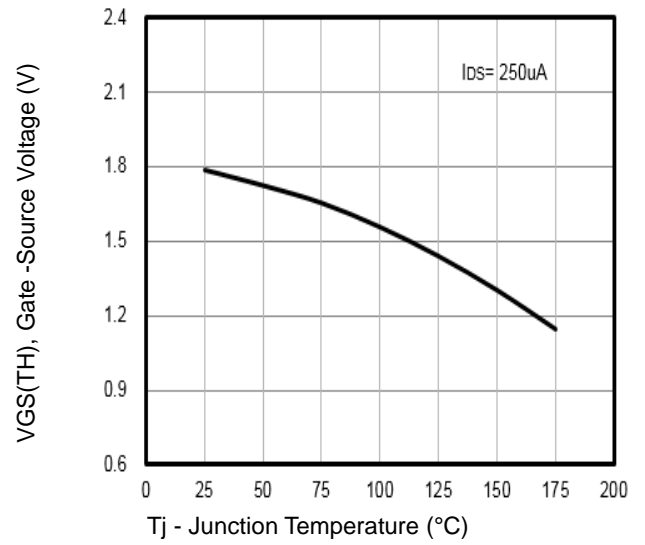


Fig2. $V_{GS(TH)}$ Gate-Source Voltage Vs. T_j

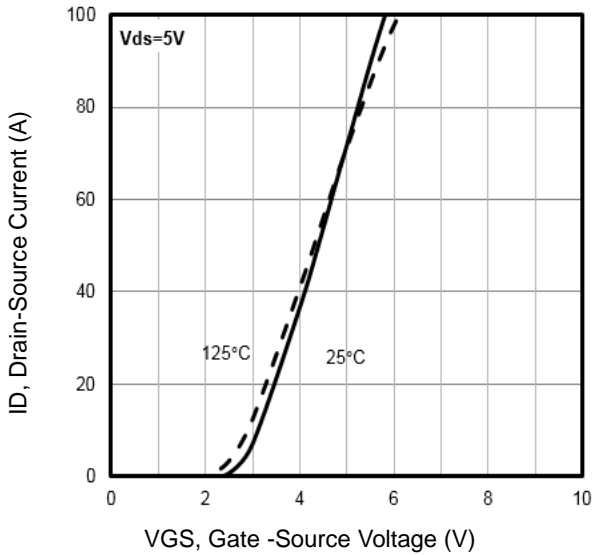


Fig3. Typical Transfer Characteristics

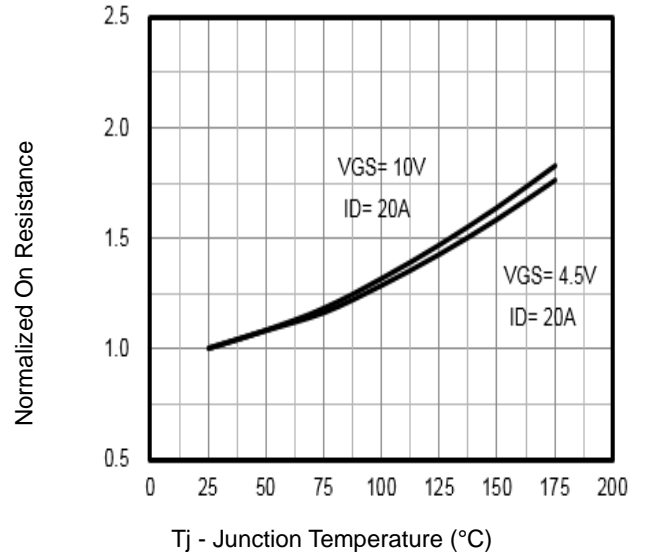


Fig4. Normalized On-Resistance Vs. T_j

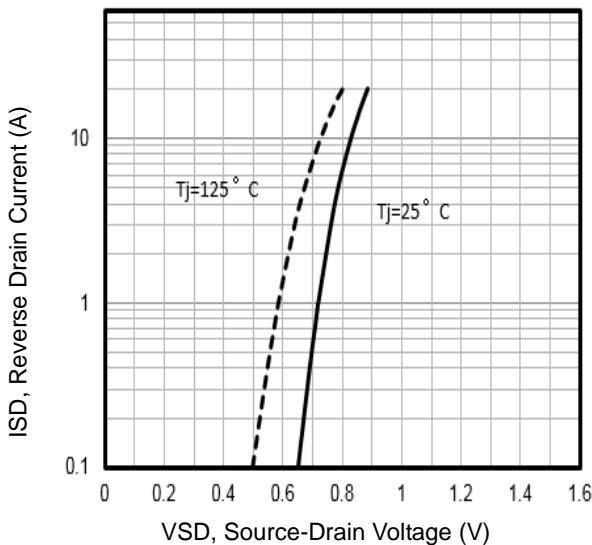


Fig5. Typical Source-Drain Diode Forward Voltage

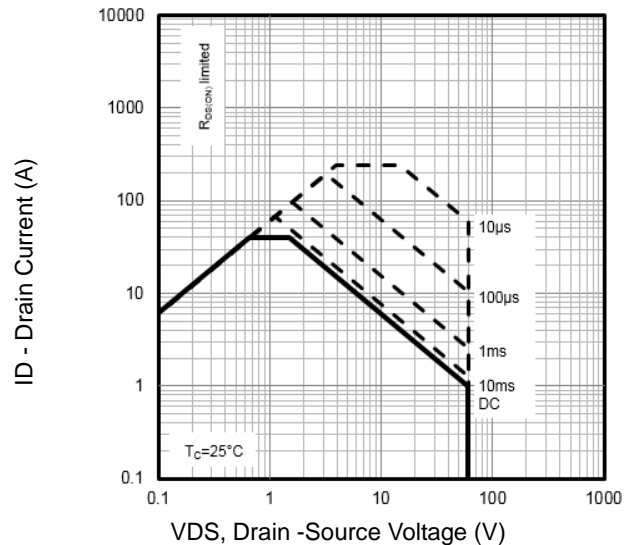


Fig6. Maximum Safe Operating Area

Typical Characteristics

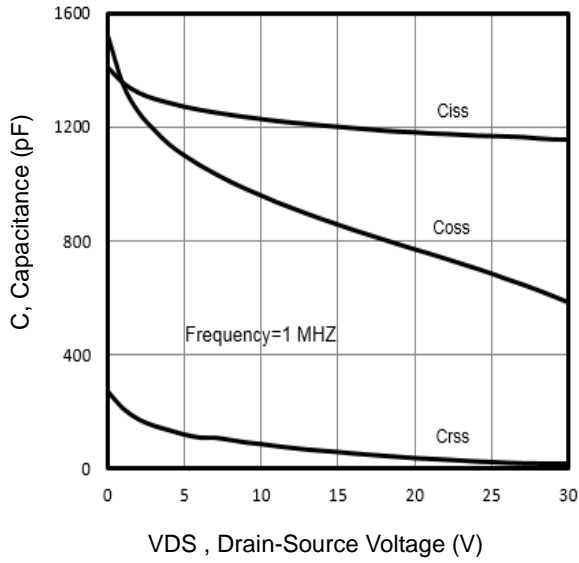


Fig7. Typical Capacitance Vs.Drain-Source Voltage

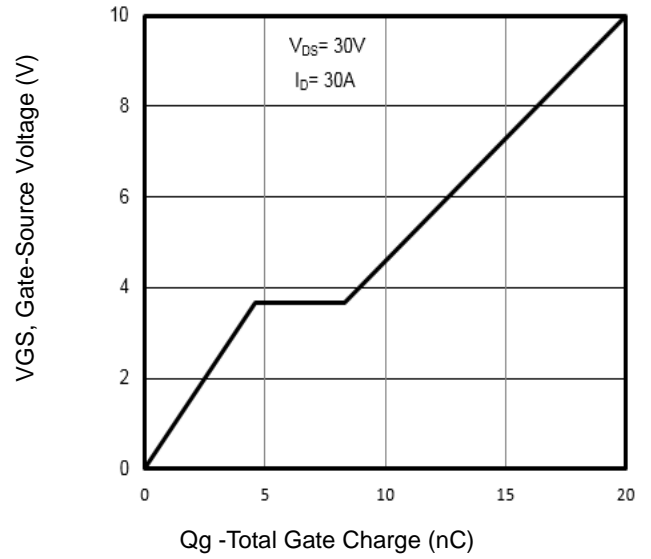


Fig8. Typical Gate Charge Vs.Gate-Source Voltage

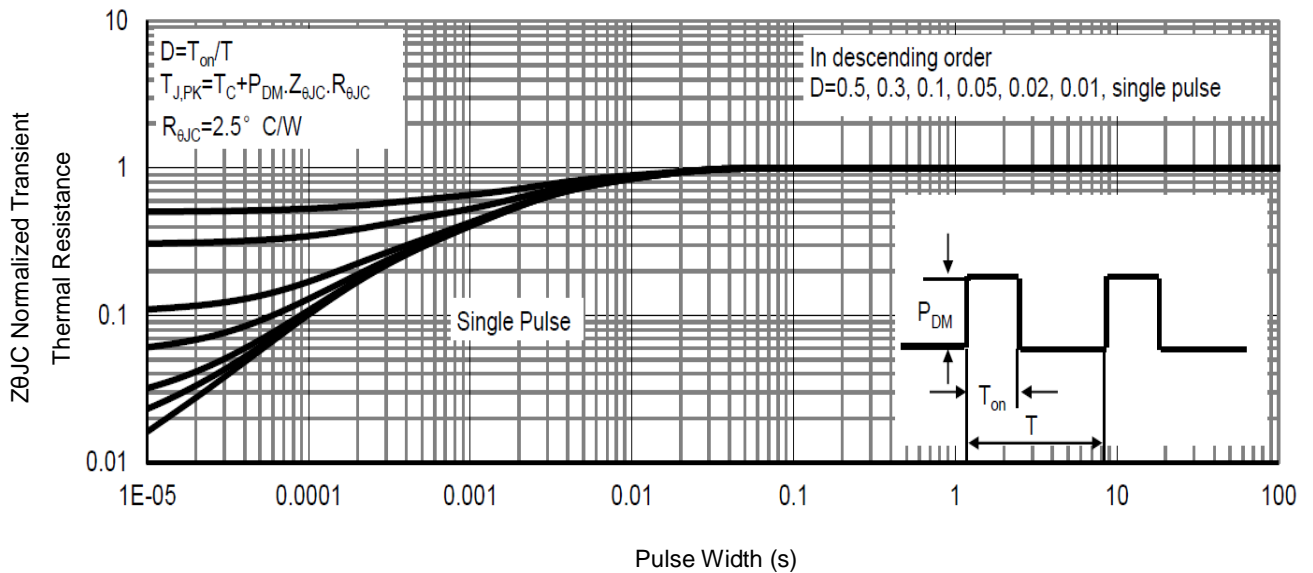


Fig9. Normalized Maximum Transient Thermal Impedance

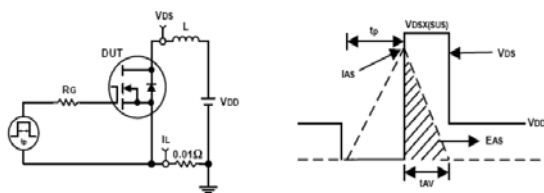


Fig10. Unclamped Inductive Test Circuit and waveforms

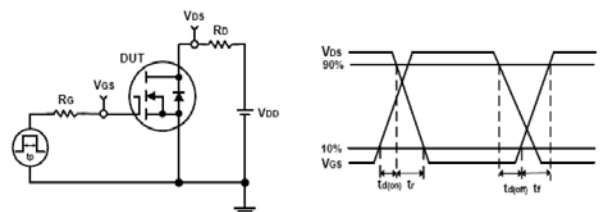
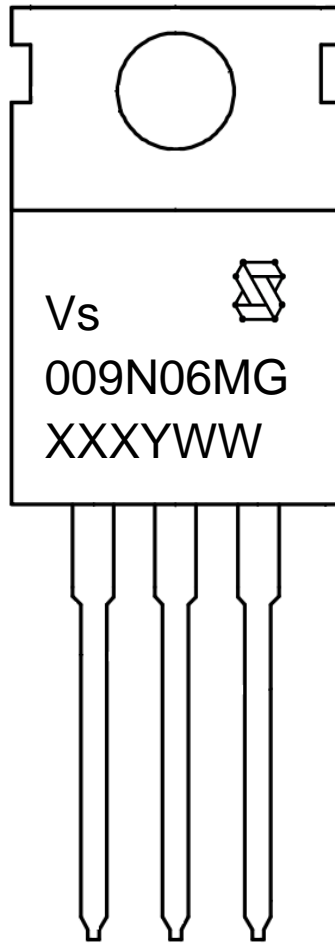


Fig11. Switching Time Test Circuit and waveforms



Marking Information



1st line: Vanguard Code (Vs), Vanguard Logo

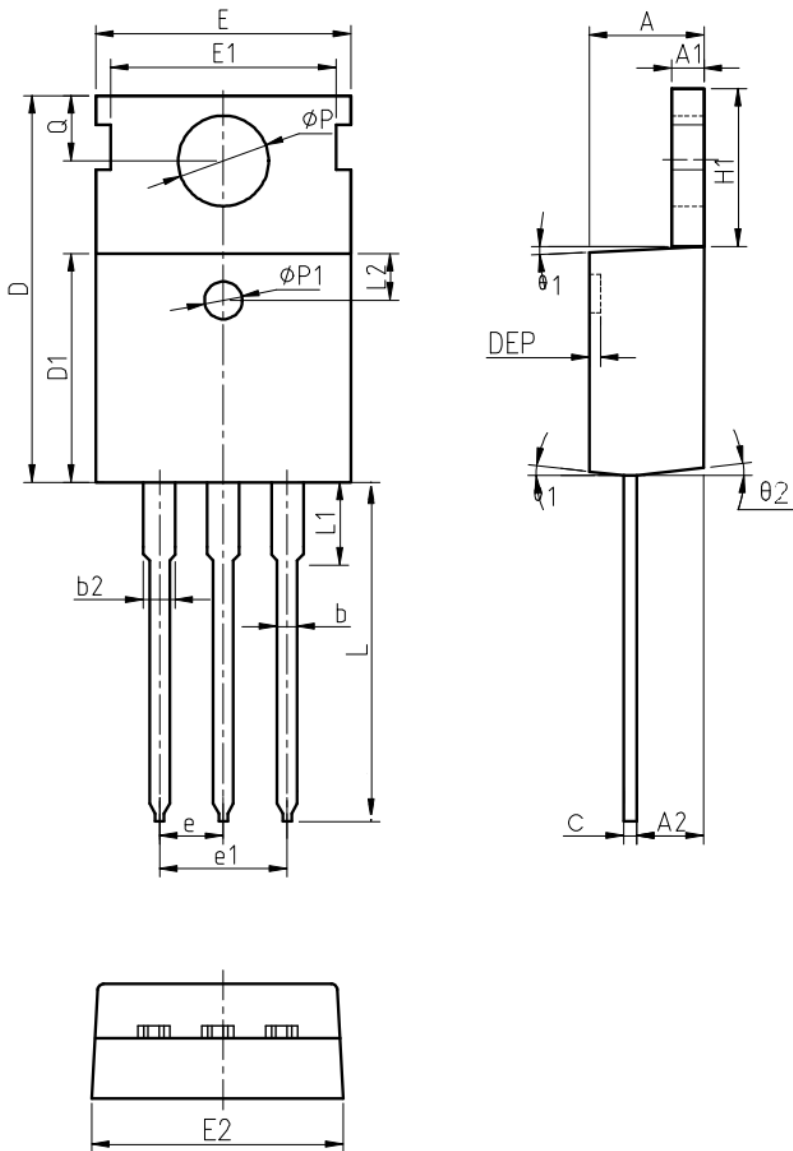
2nd line: Part Number (009N06MG)

3rd line: Date code (XXXYWW)

XXX: Wafer Lot Number Code , code changed with Lot Number

Y: Year Code, (e.g. E=2017, F=2018, G=2019, H=2020, etc)

WW: Week Code (01 to 53)

TO-220AB Package Outline Data


Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	4.30	4.52	4.70
A1	1.15	1.30	1.40
A2	2.20	2.40	2.60
b	0.70	0.80	1.00
b2	1.17	1.32	1.50
c	0.45	0.50	0.61
D	15.30	15.65	15.90
D1	9.00	9.20	9.40
DEP	0.05	0.10	0.25
E	9.66	9.90	10.28
E1	-	8.70	-
E2	9.80	10.00	10.20
$\phi P1$	1.40	1.50	1.60
e	2.54 BSC		
e1	5.08 BSC		
H1	6.40	6.50	6.80
L	12.70	-	14.27
L1	-	-	3.95
L2	2.40	2.50	2.60
ϕP	3.53	3.60	3.70
Q	2.70	2.80	2.90
$\theta 1$	5 °	7 °	9 °
$\theta 2$	1 °	3 °	5 °

Notes:

1. Refer to JEDEC TO-220 variation AB
2. Dimension "D" and "E" do NOT include mold flash. Mold flash shall not exceed 0.127mm per side.

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